# Deltaflow.Control: A distributed control system architecture for large-scale ion trap and cold atom quantum computing

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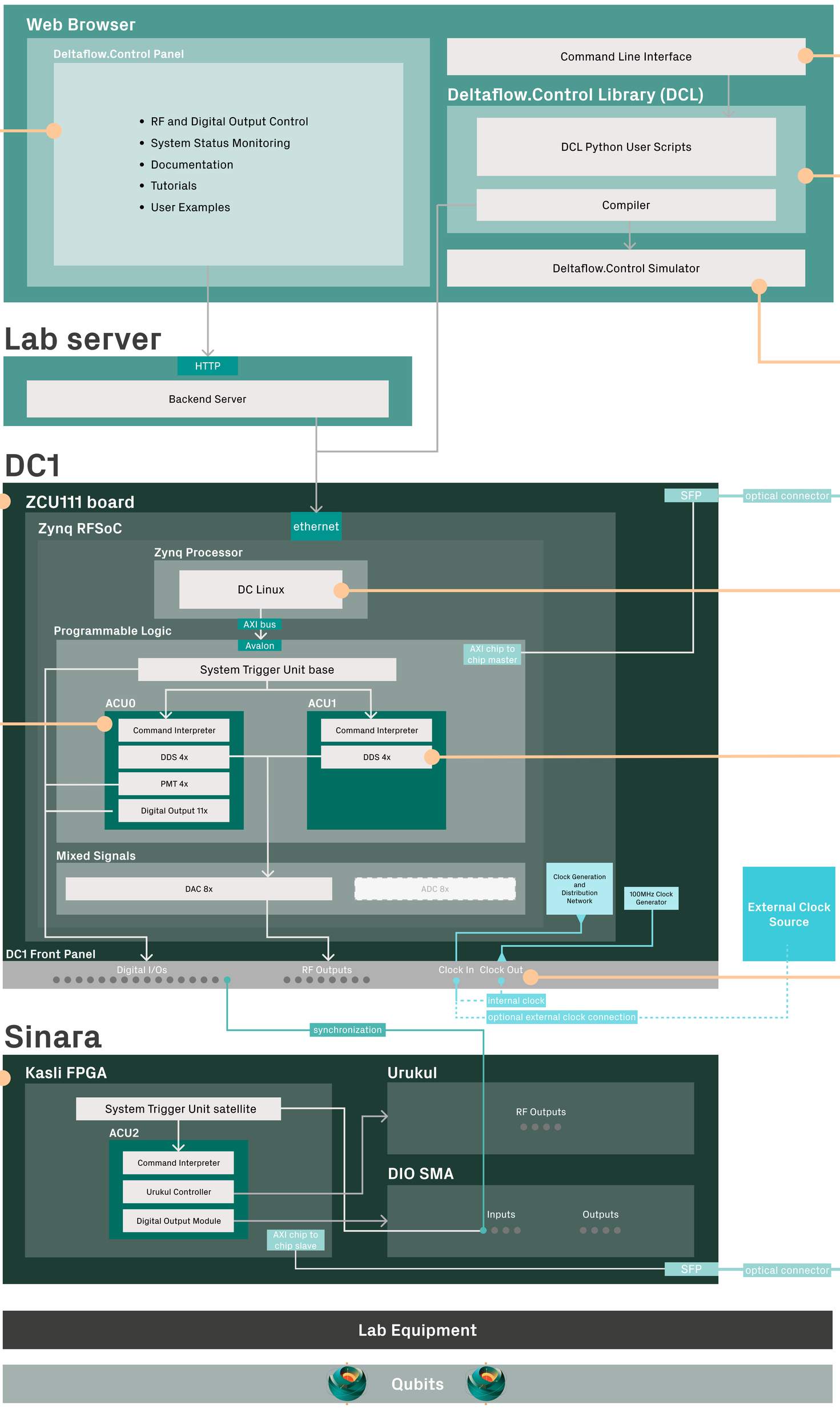
**Abstract**

A dedicated control system is pivotal for sophisticated experiments in atomic, molecular and optical (AMO) physics. In particular, large-scale ion-trap and neutral atom quantum computing will require some of the most complex control systems ever built. These will need to support measurement-heavy workflows, fast feedback with tight latency constraints, and be scalable in hardware and software. Here, we present the architecture of Deltaflow.Control, an FPGA-based control system designed with large-scale error-corrected quantum computing in mind. Its distributed architecture pushes processing out to all system components, reducing latency of feedback and feedforward loops. Modular atomic control units (ACUs) enable multi-tone generation of phase-coherent pulses with sub-nanosecond accuracy. We show bottleneck-free execution of instructions on all channels with scalability to multiple FPGAs and larger heterogeneous systems. Finally, we present an intuitive and deterministic programming model and a user interface for quick control, tune up and experiment orchestration crucial to saving time in the lab and enabling further advances. Our goal is to provide a powerful control system that can handle the growing list of requirements for error-corrected, large-scale quantum computing.

**Deltaflow.Control Panel**
The Control Panel is implemented as a locally hosted web application and can be easily accessed anywhere in the lab, or from outside the lab via a VPN. Users can toggle Digital Outputs and RF Outputs, and monitor system status directly via the Control Panel, which communicates with the FPGA via the Backend server.




**Command Line Interface**
Deltaflow.Control can also be controlled via the command line which mirrors the functionality of the Control Panel and exposes additional features like experiment execution.

**Deltaflow.Control Library**
The Deltaflow.Control Library (DCL) is a Python library through which the user can program the control system. DCL scripts are compiled directly into code executable by the FPGA with meaningful error messages, and executed in a fully time-deterministic way. The same scripts can also be compiled and executed on the Deltaflow.Control Simulator.

**Deltaflow.Control Simulator**
The DC simulator is architected such that the same DCL scripts can be executed in simulation mode and on real hardware. The simulation operates at clock-cycle level accuracy showing the exact hardware behavior. The simulator VCD can be visualized in third-party software such as GTKWave.

**DC1**
The DC1 sits at the heart of Deltaflow.Control. Powered by the Xilinx RFSoC ZCU111, it provides both RF and digital outputs alongside additional interfaces for future expansion and connectivity. The main system outputs are exposed on the DC1 front panel, Sinara modules can be connected at the back via SFP.

**DC Linux**
The DC Linux manages requests from the DCL and drives (“housekeeps”) the FPGA firmware providing control for the quantum system.

**Atomic Control Unit (ACU)**
The ACU is a container for customizable hardware blocks. It pushes the processing and logic right to the periphery of the system and allows the control system architecture to be customized to the requirements of each lab. In the current architecture there are two ACUs on the main ZCU111 board and one ACU on the Sinara Kasli FPGA.

**Direct Digital Synthesis (DDS) module**
A DDS module is used to generate precise and stable digital waveforms. It consists of a phase accumulator, a lookup table and works with a high-speed digital-to-analog converter (DAC). The phase accumulator accumulates phase increments at a specified frequency, while the lookup table converts the accumulated phase values into corresponding digital samples. These samples are then converted to analog signals by the DAC, producing a continuous waveform with adjustable frequency, phase, and amplitude.

**Clocking**
Deltaflow.Control is powered by a single low-jitter internal 100MHz clock or can be connected to an external clock source via the Clock In pin on the DC1 front panel. Using a single clock source distributed into all computational units allows us to achieve a less than 200ps synchronization across channels on a single board and removes the need for phase alignment and drift compensation necessary with multiple clock sources.

**Sinara**
The Deltaflow.Control architecture is ported on Sinara’s Kasli FPGA exposing an additional ACU to the user. The ACU is composed of the same command interpreter to send timing accurate instructions, the same digital output module for connecting Sinara’s DIO SMA, and the Sinara-specific Urukul controller for connecting the Urukul card to the Kasli. The reconfigurability of the ACU is leveraged to maintain the processing power at the periphery on a different piece of hardware while maintaining scalability and usability. The Kasli FPGA can be programmed at the user level in the same way as the DC1 via the Deltaflow.Control Library.